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SPECIFICATION

VXT700YIA-02C

☐ Preliminary Specification

☐ Final Specification

Made By:
Checked By:
Approved By:
Quality:
Date:
Note:

Approved By:
Date:
Note:

Date	Rev.No.	Page	Revision Items	Prepared
2023-10-19	V00		The first release	solon
2024-11-04	V01	4,5	Update the VA of CTP.	solon
2024-11-06	V02	8	Add power consumption description	solon

3. General Specifications

VXT700YIA-02C is a TFT-LCD module. It is composed of a TFT-LCD panel, driver IC, FPC, a back light and CTP . The 7.0″ display area contains 800 x (RGB) x 1280 pixels and can display up to 16.7M colors. This product accords with ROHS environmental criterion..

3.1 LCD Parameter

Item	Contents	Unit	Note
LCD Type	TFT	-	
Display color	16.7M	-	1
Viewing Direction	ALL	O'Clock	
Operating temperature	-20 ~ +60	℃	
Storage temperature	-30 ~ +70	℃	
Module size	Refer to outline drawing	mm	2
Active Area(W×H)	94.20 X 150.72	mm	
Number of Dots	800 X 1280	dots	
TFT Controller	ILI9881	-	
Power Supply Voltage	3.3	V	
Outline Dimensions	Refer to outline drawing	-	
Backlight	5S4P-LEDs	pcs	
Weight	---	g	
Interface	MIPI	-	

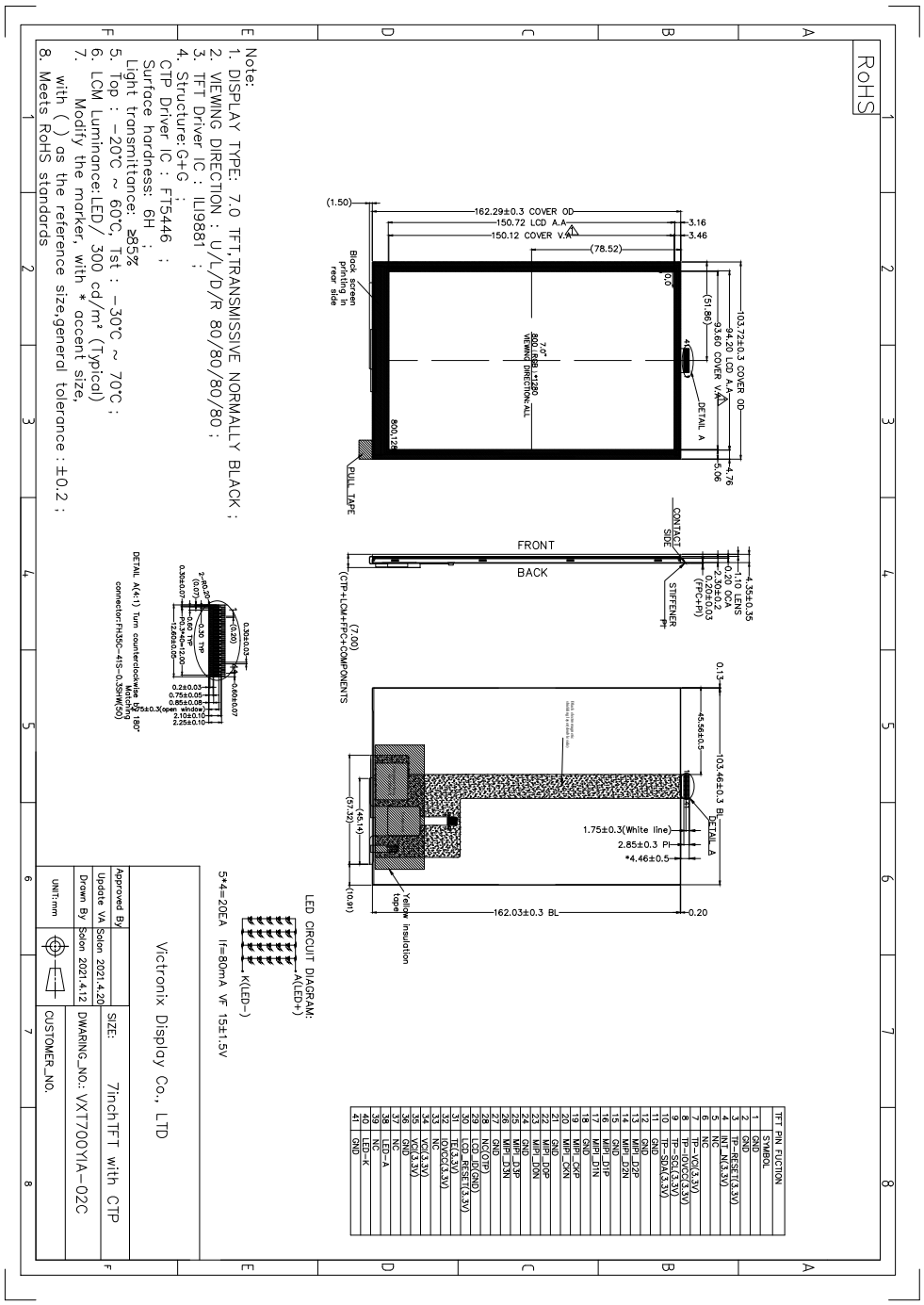
Note 1: Color tune is slightly changed by temperature and driving voltage.

Note 2: Without FPC and Solder.

3.2 CTP Parameter

Item	Contents	Unit	Note
Outline Size	103.72(H)X162.29(V)X1.10(T)	mm	
Cover View Area	95.20(H)X151.72(V)		
CTP Resolution	800 X 1280	dots	
Interface Mode	IIC	-	
Touch Mode	10 Human fingers multi-touch	-	
Surface hardness	>=6H	-	
Transparency	>=86%	-	
Accuracy	Entre +/-1.5mm,Edge +/-2.5mm	mm	
CTP Controller	FT5446	-	
Power Supply Voltage	3.3	V	

4.Outline.Drawing



5. Absolute Maximum Ratings(Ta=25℃)

5.1 Electrical Absolute Maximum Ratings.(Vss=0V ,Ta=25℃)

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VCC	-0.3	6.5	V	1，2
Power Supply Voltage	IOVDD	-0.3	3.8	V	
CTP Power Supply Voltage	VDD	2.8	3.3	V	1，2

Notes:

1. If the module is above these absolute maximum ratings. It may become permanently damaged. Using the module within the following electrical characteristic conditions are also exceeded, the module will malfunction and cause poor reliability.
2. V_{DDIN} >V_{SS} must be maintained.
3. Please be sure users are grounded when handing LCD Module.

5.2 Environmental Absolute Maximum Ratings.

Item	Storage		Operating		Note
	MIN.	MAX.	MIN.	MAX.	
Ambient Temperature	-30℃	70℃	-20℃	60℃	1,2
Humidity	-	-	-	-	3

1. The response time will become lower when operated at low temperature.
2. Background color changes slightly depending on ambient temperature.
   The phenomenon is reversible.
3. Ta<=40℃:85%RH MAX.
   Ta>=40℃:Absolute humidity must be lower than the humidity of 85%RH at 40℃.

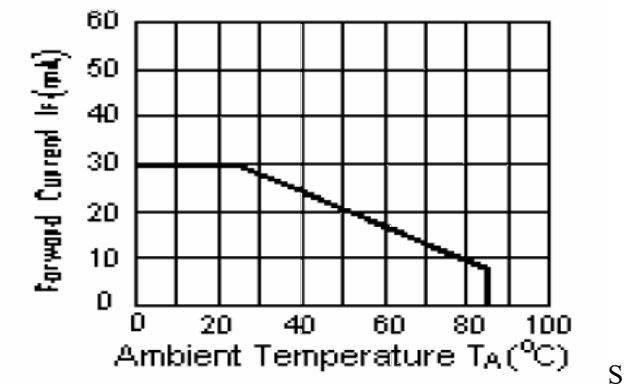
6. Electrical Specifications

6.1 Electrical characteristics for LCD(Vss=0V ,Ta=25℃)

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Note
Power supply		VCC	Ta=25℃	2.6	3.3	3.6	V	
Power supply		IOVDD	Ta=25℃	1.65	3.3	3.6	V	
Input voltage	'H'	V_{IH}	V_{CC}=1.8V	0.7V_{CC}	-	V_{CC}	V	
	'L'	V_{IL}	V_{CC}=1.8V	0	-	0.3V_{CC}	V	
Current consumption		I_{VCC}	Ta=25℃	-	52.1	-	mA	包含 I_{VCC}，I_{IOVDD}
Power consumption		P_{TFT}		-	171.9	-	mW	
		P_{CTP}		-	50.49	-	mW	
		P_{BL}		-	450	-	mW	

6.2.LED backlight specification(VSS=0V ,Ta=25℃)

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply voltage	Vf	If=80mA	13.5	15.0	16.5	V	
Uniformity	ΔBp	If=80mA	75	80	-	%	
Life Time	time	If=80mA	20K	-	-	hours	1



S

Note 1: Brightness to be decreased to 50% of the initial value at ambient temperature TA=25℃

6.3 Interface signals

6.3.1 LCM PIN

Pin No.	Symbol	I/O	Function
1-2	GND	P	Ground.
3	TP-RESET(3.3V)	I	CTP reset pin
4	INT_N(3.3V)	I	External Interrupt to the IC of CTP
5-6	NC		No connection.
7	TP-VCI(3.3V)	P	CTP Analog or digital supply voltage
8	TP-IOVCC(3.3V)	P	CTP I/O circuit or logic supply voltage
9	TP-SCL(3.3V)	I	CTP Serial interface clock pin
10	TP-SDA(3.3V)	I	CTP Serial in/out signal pin
11-12	GND	P	Ground.
13	MIPI_2P	I	MIPI-DSI Data differential signal input pins. (Data lane 2).
14	MIPI_2N	I	MIPI-DSI Data differential signal input pins. (Data lane 2).
15	GND	P	Ground.
16	MIPI_1P	I	MIPI-DSI Data differential signal input pins. (Data lane 1).
17	MIPI_1N	I	MIPI-DSI Data differential signal input pins. (Data lane 1).
18	GND	P	Ground.
19	MIPI_CLKP	I	MIPI-DSI CLK differential signal input pins.
20	MIPI_CLKN	I	MIPI-DSI CLK differential signal input pins.
21	GND	P	Ground.
22	MIPI_0P	I	MIPI-DSI Data differential signal input pins. (Data lane 0).
23	MIPI_0N	I	MIPI-DSI Data differential signal input pins. (Data lane 0).
24	GND	P	Ground.
25	MIPI_3P	I	MIPI-DSI Data differential signal input pins. (Data lane 3).
26	MIPI_3N	I	MIPI-DSI Data differential signal input pins. (Data lane 3).
27	GND	P	Ground.
28	NC(OTP)		No connection.
29	LCD_ID(GND)	I	ID select pin
30	LCD_RESET(3.3V)	I	Global reset signal input pin
31	TE(3.3V)	I	Serves TE(Tearing Effect) pin
32	IOVCC(3.3V)	P	I/O circuit or logic supply voltage
33	NC		No connection.
34-35	VCI(3.3V)	P	Power supply(3.3V).
36	GND	P	Ground.
37	NC		No connection.
38	LED-A	P	LED back light(Anode).
39	NC		No connection.
40	LED-K	P	LED back light(Cathode).
41	GND	P	Ground.

6.4 AC Characteristics

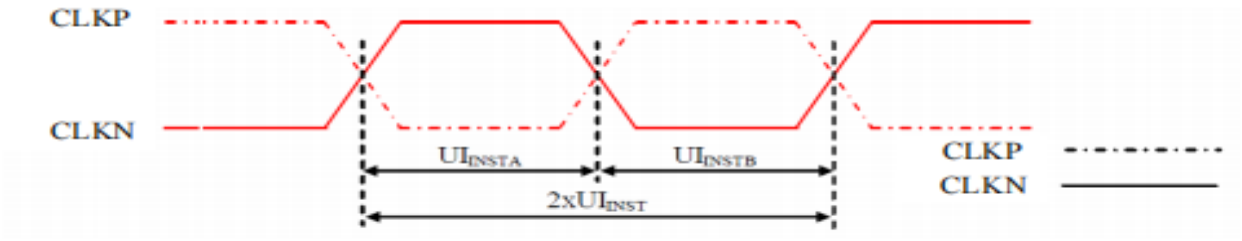


Figure 118: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
CLKP/N	UI_{INSTA},UI_{INSTB} (Note 1)	UI instantaneous Half	2 (Note 2)	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value of 24 UI per Pixel, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	433 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	487 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps

High Speed Mode – Data Clock Channel Timing

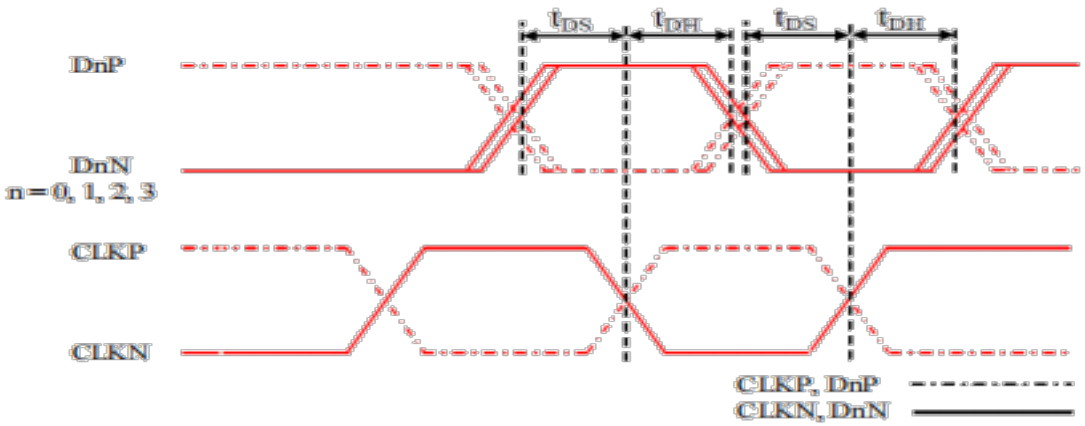
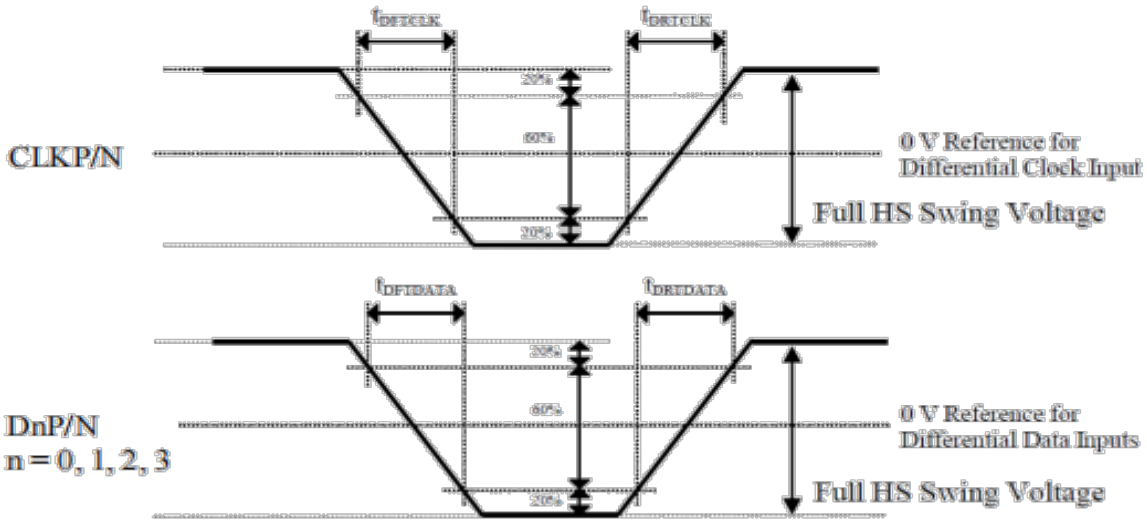


Figure 119: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N ,n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	–
	t_{DH}	Clock to Data Hold Time	0.15xUI	–

High Speed Mode – Rising and Falling Timings



Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.

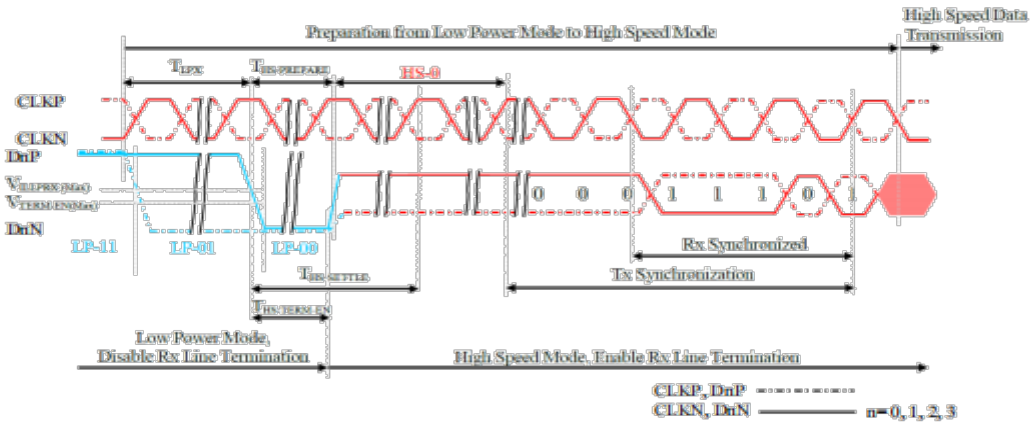


Figure 123: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

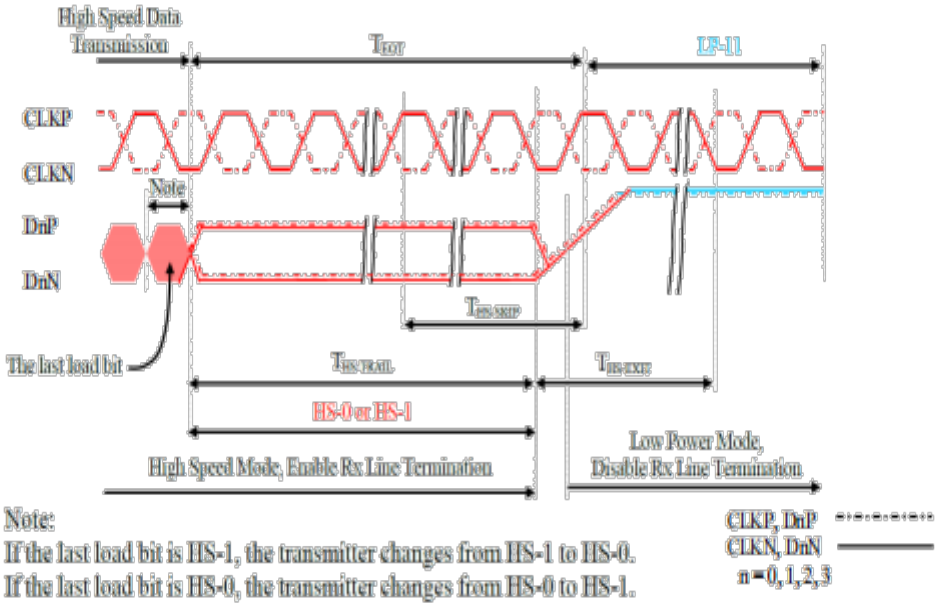


Figure 124: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

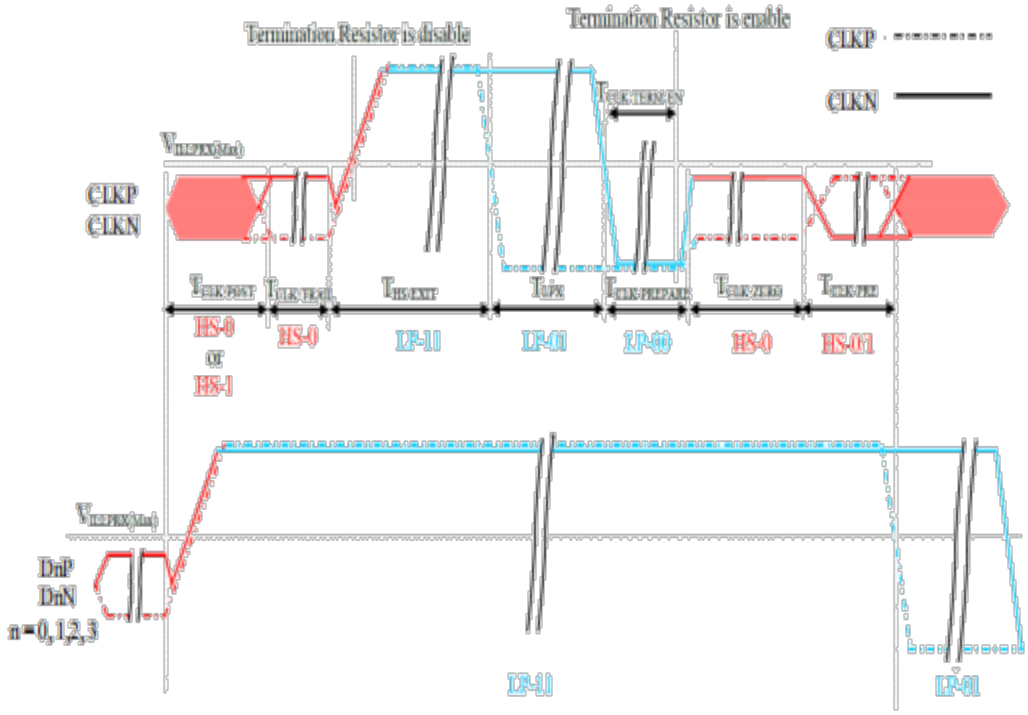


Figure 125: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

6.5 Reset input timings

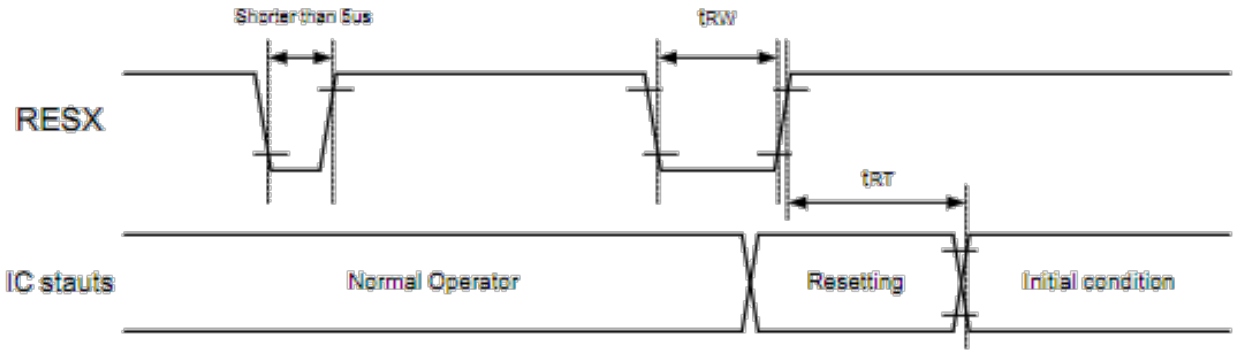


Figure 11.1: Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset pulse width[2]	RESX	10	-	µs
t_{RT}	Reset complete time[3]	-	-	5 (Note 5)	ms
		-	-	120 (Note 6, 7)	ms

Note: (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

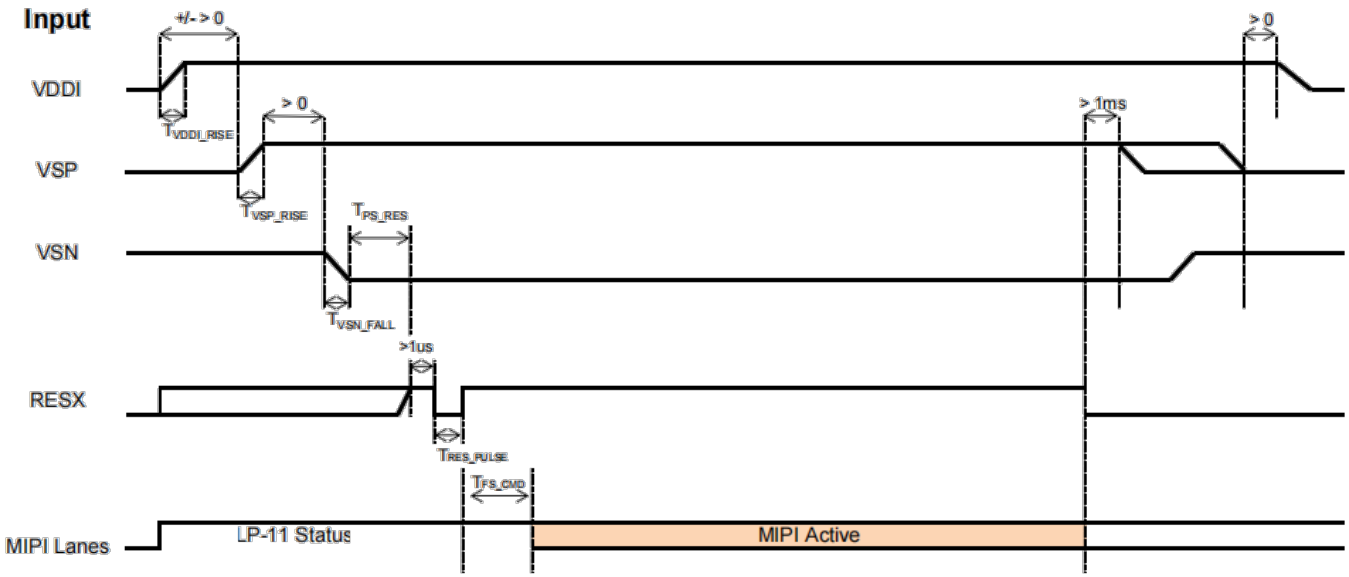
RESX Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:

6.6 Power on/off Sequence

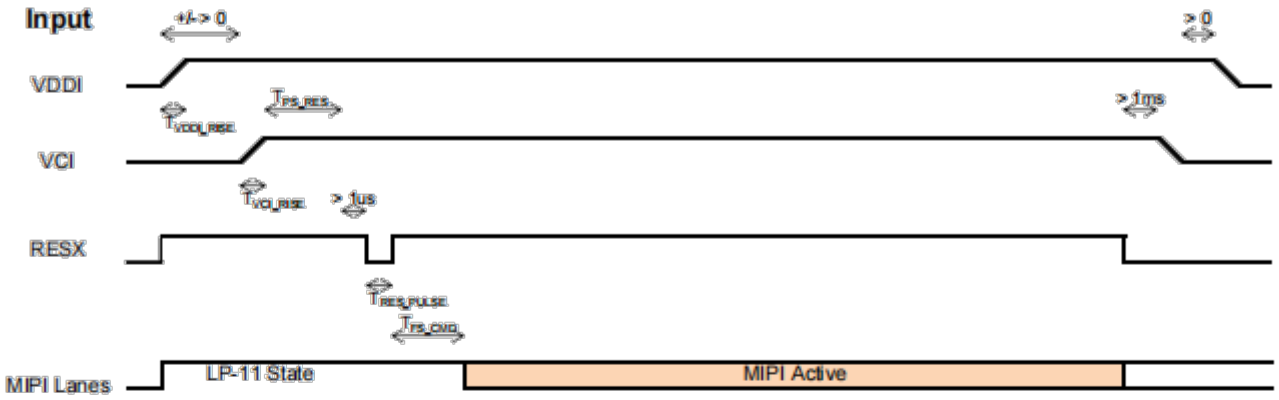
6.6.1 Power Mode 2A



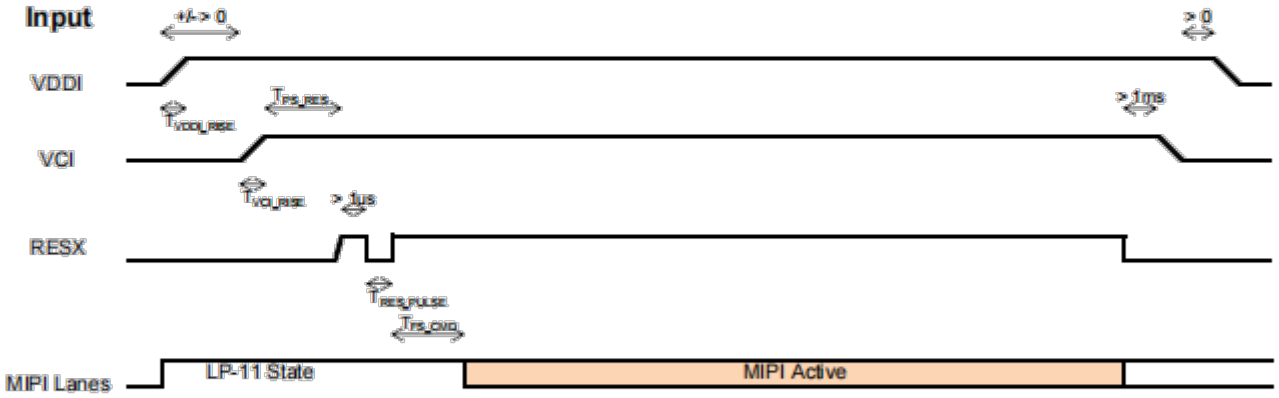
Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VSP_RISE}	VSP Rise time	130	-	-	us
T_{VSN_FALL}	VSN Fall time	200	-	-	us
T_{PS_RES}	VDDI/VSP on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

6.6.2 Power Mode 3

Case A:

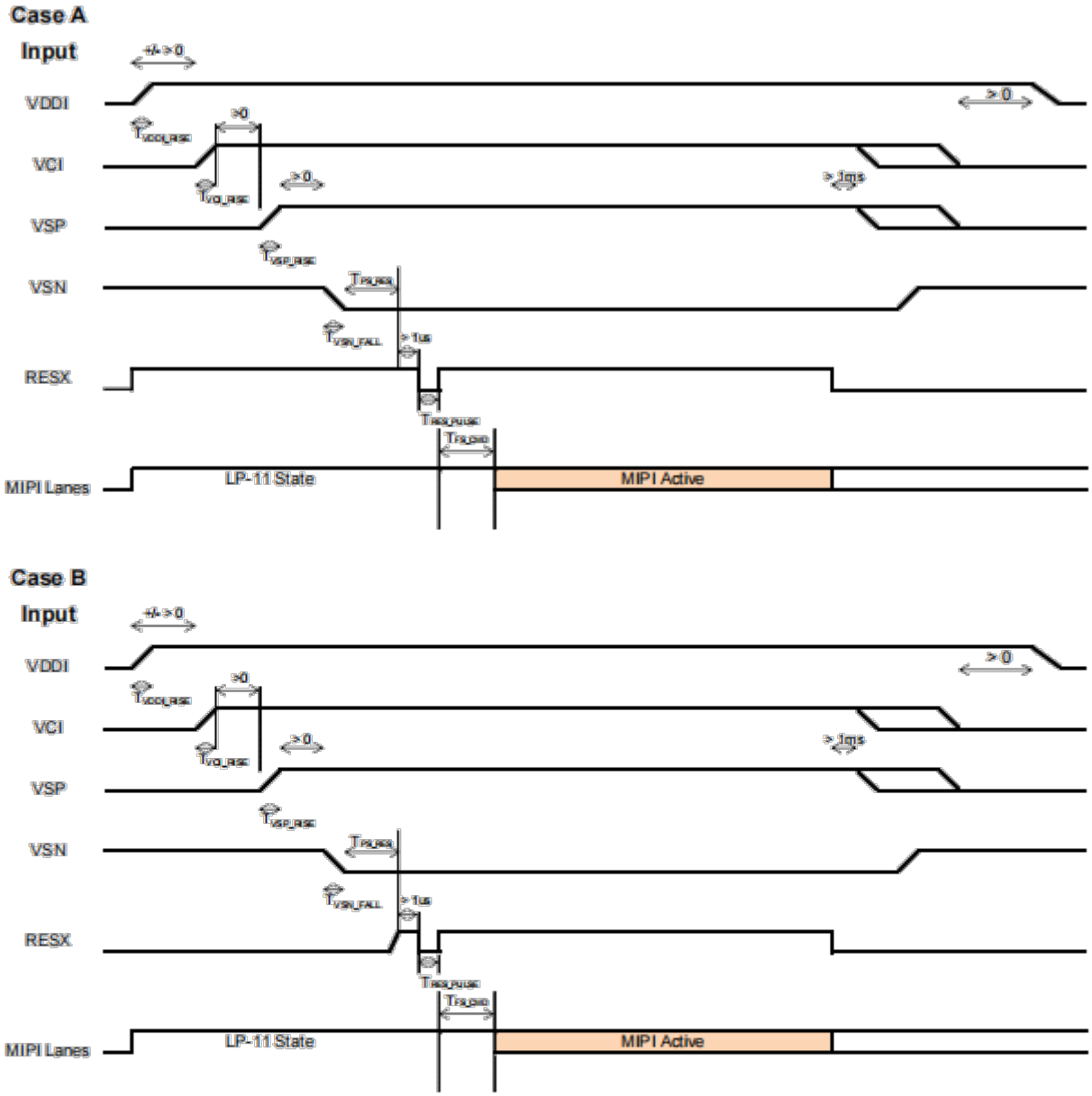


Case B:



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VCI_RISE}	Case A: VCI Rise time	130	-	-	us
	Case B: VCI Rise time	40			
T_{PS_RES}	VDDI/VCI on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

6.6.3 Power Mode 4



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VCI_RISE}	Case A: VCI Rise time	130	-	-	us
	Case B: VCI Rise time	40			
T_{VSP_RISE}	VSP Rise time	130	-	-	us
T_{VSN_FALL}	VSN Fall time	200	-	-	us
T_{PS_RES}	VDDI/VCI on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

7. Optical Characteristics

Item	Symbol		Condition	Min.	Typ.	Max.	Unit	Note
Brightness	Bp		θ=0° F=0°	-	300	-	Cd/m^2	1
Uniformity	⊿Bp			75	80	-	%	1,2
Viewing Angle	3:00		Cr≥10	-	80	-	Deg	3
	6:00			-	80	-		
	9:00			-	80	-		
	12:00			-	80	-		
Contrast Ratio	Cr		*Ta*=25℃CF=0°	800	1000	-	-	4
Response Time	$T_{r+}T_f$			-	25	35	ms	5
Color of CIE Coordinate	W	x	θ=0° F=0°	Typ -0.05	0.305	Typ +0.05	-	1,6
		y			0.345		-	
	R	x			0.596		-	
		y			0.361		-	
	G	x			0.330		-	
		y			0.581		-	
	B	x			0.147		-	
		y			0.119		-	
NTSC Ratio	S			-	50	-	%	

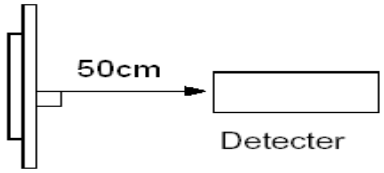
Note：The parameter is slightly changed by temperature, driving voltage and materiel

Note 1: The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment BM-7 (Φ5mm)

Measuring condition:

- Measuring surroundings: Dark room.
- Measuring temperature: Ta=25℃.
- Adjust operating voltage to get optimum contrast at the center of the display.

Measured value at the center point of LCD panel after more than 5 minutes while backlight turning on.

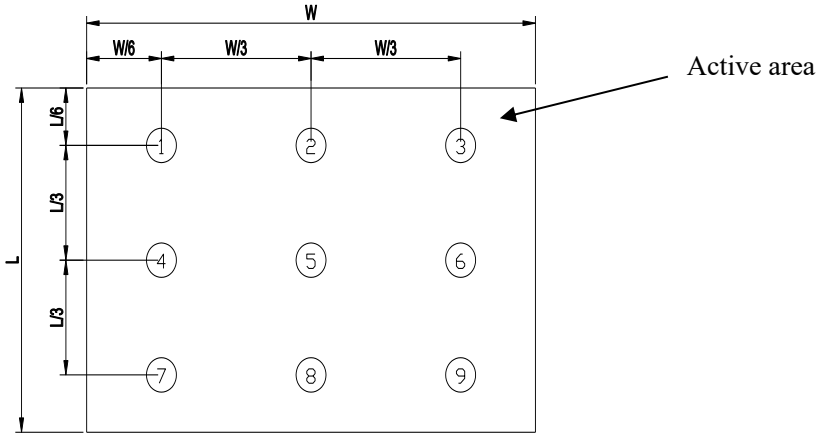


Note 2: The luminance uniformity is calculated by using following formula.

⊿Bp = Bp (Min.) / Bp (Max.)×100 (%)

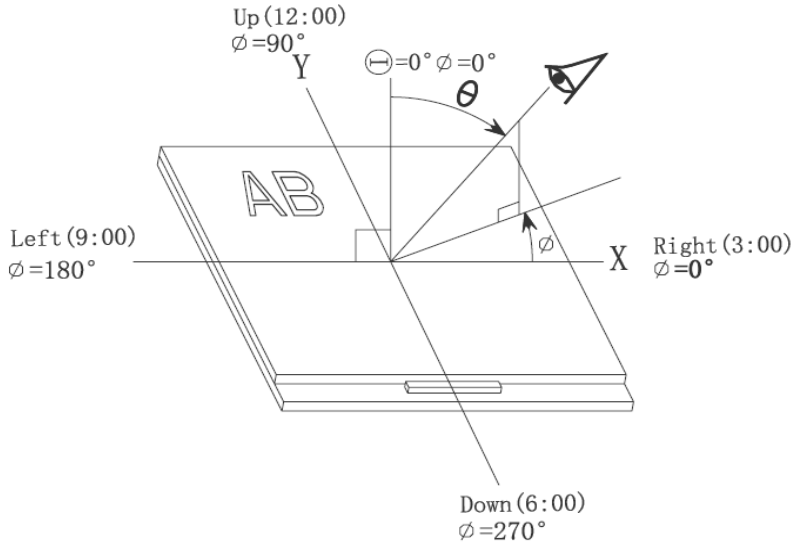
Bp (Max.) = Maximum brightness in 9 measured spots

Bp (Min.) = Minimum brightness in 9 measured spots.

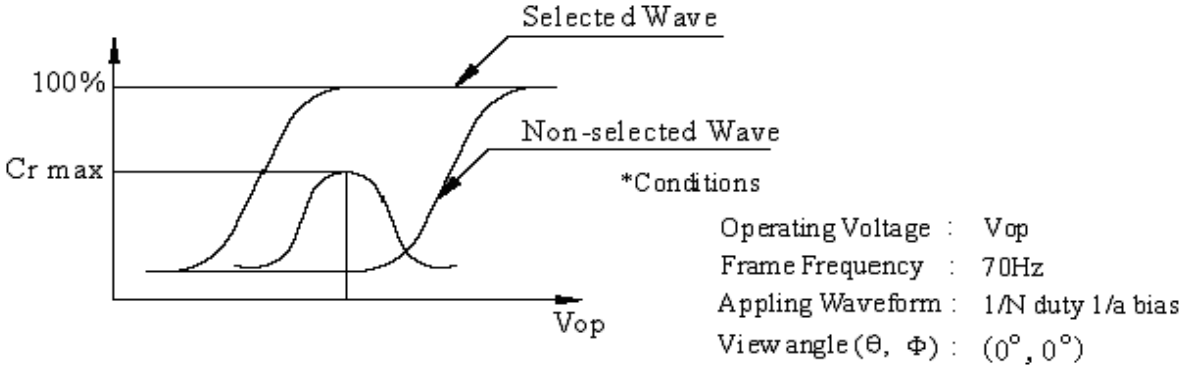


Note 3: The definition of viewing angle:

Refer to the graph below marked by θ and Φ



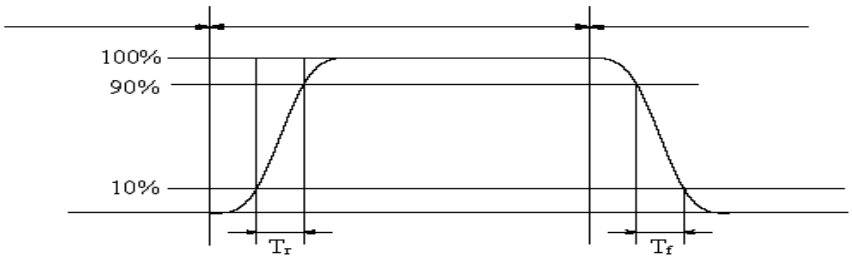
Note 4: Definition of contrast ratio.(Test LCD using DMS501)



$$Contrast\ ratio(Cr) = \frac{Brightness\ of\ selected\ dots}{Brightness\ of\ non-selected\ dots}$$

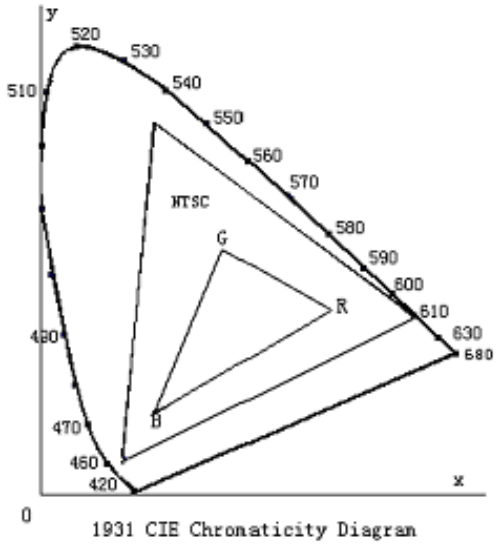
Note 5: Definition of Response time. (Test LCD using DMS501):

The output signals of photo detector are measured when the input signals are changed from“black”to“white”(falling time) and from“ white”to “black”(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes.Refer to figure as below.



The definition of response time

Note 6: Definition of Color of CIE Coordinate and NTSC Ratio.

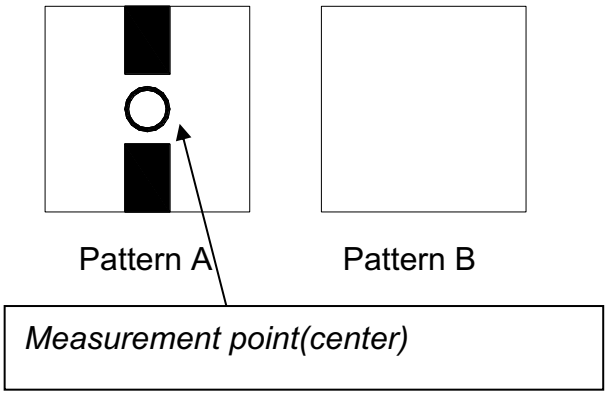


1931 CIE Chromaticity Diagram

Color gamut:

$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 7: Definition of cross talk.
Cross talk ratio(%)=|pattern A Brightness-pattern B Brightness|/pattern A Brightness*100



Electric volume value=3F+/-3Hex

8. Reliability Test Items and Criteria

Test Item	Test condition	Remark
High Temperature Storage	Ta = 70℃ 96hrs	Note1,Note3,4
Low Temperature Storage	Ta = -30℃ 96hrs	Note1,Note3,4
High Temperature Operation	Ts = 60℃ 96hrs	Note2,Note3,4
Low Temperature Operation	Ta = -20℃ 96hrs	Note1,Note3,4
Operation at High Temperature/Humidity	+60℃, 90%RH 96hrs	Note3,4
Thermal Shock	-20℃/30 min ~ +60℃/30 min for a total 100 cycles, Start with cold temperature and end with high temperature.	Note3,4

Note 1: Ta is the ambient temperature of samples.

Note 2: Ts is the temperature of panel's surface.

Note 3: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

Note 4: Before cosmetic and function test, the product must have enough recovery time,at least 2 hours at room temperature

9. Precautions for Use of LCD Modules

9.1 Handling Precautions

9.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

9.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

9.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

9.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

9.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

— Isopropyl alcohol — Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

— Water — Ketone — Aromatic solvents

9.1.6 Do not attempt to disassemble the LCD Module.

9.1.7 If the logic circuit power is off, do not apply the input signals.

9.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

a. Be sure to ground the body when handling the LCD Modules.

b. Tools required for assembly, such as soldering irons, must be properly ground.

c. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

d. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

9.2 Storage precautions

9.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

9.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃

Relatively humidity: ≤ 80%

9.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

9.3 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

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